09/917,238

L Number	Hits	Search Text	DB	Time stamp
1	2667	phase adj1 alignment	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 09:18
2	141374	multiplexer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 09:20
3	83	(phase adj1 alignment) same multiplexer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 09:20
4	17	sampl$3 same ((phase adj1 alignment) same multiplexer)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 09:37
5	9035	clock near2 recovery	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 10:10
6	335	(phase adj1 alignment) and (clock near2 recovery)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 10:10
7	304761	oscillator	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 10:10
8	3708	barrel adj2 shift$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 10:10
9	5	((phase adj1 alignment) and (clock near2 recovery)) and oscillator and (barrel adj2 shift$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:04
10	2	6414523.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:06
11	2	(phase adj1 alignment) same (barrel adj2 shift$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:07
12	27	(phase adj1 alignment) and (barrel adj2 shift$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:16
13	8	(barrel adj2 shift$3) and ((phase adj1 alignment) same multiplexer)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:18
14	1		USPAT	2004/10/27 11:18
15	1		USPAT	2004/10/27 11:18
16	968	pulse adj1 width adj1 adjust$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:19
17	1400	pulse adj1 width adj1 adjust$4	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:19
18	2	(phase adj1 alignment) and (pulse adj1 width adj1 adjust$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:20

19	131	(pulse adj1 width adj1 adjust$4) and multiplexer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:20
20	1	((pulse adj1 width adj1 adjust$4) and multiplexer) and (barrel adj2 shift$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:20
21	1	((pulse adj1 width adj1 adjust$4) and multiplexer) and (clock near2 recovery)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:20
22	31	((phase adj1 alignment) same multiplexer) and (clock near2 recovery)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:29
23	19	(phase adj1 alignment) and multiplexer and (barrel adj2 shift$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:29

Your search matched **9** of **1085387** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descend** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new or the text box.

clock<and>recovery<paragraph> phase<and>alignmer Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Single-chip 1062 Mbaud CMOS transceiver for serial data communication**
Ewen, J.F.; Widmer, A.X.; Soyuer, M.; Wrenner, K.R.; Parker, B.; Ainspan, H.A.;
Solid-State Circuits Conference, 1995. Digest of Technical Papers. 42nd ISSCC, 1995 IE International , 15-17 Feb. 1995
Pages:32 - 33, 336

[Abstract] [PDF Full-Text (948 KB)] IEEE CNF

---

2 **Clock and data recovery circuit for 10-Gb/s asynchronous optical packets**
Kanellos, G.T.; Stampoulidis, L.; Pleros, N.; Houbavlis, T.; Tsiokos, D.; Kehayas, E.; Avramopoulos, H.; Guekos, G.;
Photonics Technology Letters, IEEE , Volume: 15 , Issue: 11 , Nov. 2003
Pages:1666 - 1668

[Abstract] [PDF Full-Text (348 KB)] IEEE JNL

---

3 **Architecture and methodology of a SoPC with 3.25Gbps CDR based SERDES an 1Gbps dynamic phase alignment**
Venkata, R.; Wong, W.; Tran, T.; Chan, V.; Hoang, T.; Lui, H.; Ton, B.; Shumurayev, S.; Lee; Shoujun Wang; Huy Ngo; Kabani, M.; Maruri, V.; Tin Lai; Tam Nguyen; Zaliznyak, A Luo; Toan Nguyen; Asaduzzaman, K.; Maangat, S.; Lam, J.; Patel, R.;
Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003 , 21-24 Sep 2003
Pages:659 - 662

[Abstract] [PDF Full-Text (398 KB)] IEEE CNF

---

4 **Design and realization of a 2.4 Gbps - 3.2 Gbps clock and data recovery circuit u deep-submicron digital CMOS technology**
Gursoy, Z.O.; Leblebici, Y.;
SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip] , 17-20 Sept

Pages:99 - 102

[Abstract] [PDF Full-Text (395 KB)] IEEE CNF

5 **A 2.5-Gb/s one-chip receiver module for gigabit-to-the-home (GTTH) system**
Soda, M.; Shiori, S.; Morikawa, T.; Tachigori, M.; Watanabe, I.; Shibutani, M.;
Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999 , 16-19 May 1999
Pages:273 - 276

[Abstract] [PDF Full-Text (396 KB)] IEEE CNF

6 **A single-chip 266 Mb/s CMOS transmitter/receiver for serial data communication**
Chen, D.-L.; Waldron, R.;
Solid-State Circuits Conference, 1993. Digest of Technical Papers. 40th ISSCC., 1993 IE International , 24-26 Feb. 1993
Pages:100 - 101, 269

[Abstract] [PDF Full-Text (448 KB)] IEEE CNF

7 **A 20-Gb/s CMOS multichannel transmitter and receiver chip set for ultra-high-resolution digital displays**
Fukaishi, M.; Nakamura, K.; Heiuchi, H.; Hirota, Y.; Nakazawa, Y.; Ikeno, H.; Hayama, H. Yotsuyanagi, M.;
Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 11 , Nov. 2000
Pages:1611 - 1618

[Abstract] [PDF Full-Text (192 KB)] IEEE JNL

8 **A 20 Gb/s CMOS multi-channel transmitter and receiver chip set for ultra-high resolution digital display**
Fukaishi, M.; Nakamura, K.; Heiuchi, H.; Hirota, Y.; Nakazawa, Y.; Ikeno, H.; Hayama, H. Yotsuyanagi, M.;
Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 2000 IEEE International , 7-9 Feb. 2000
Pages:260 - 261, 463

[Abstract] [PDF Full-Text (340 KB)] IEEE CNF

9 **SONET requirements for jitter interworking with existing networks**
Nunn, R.O.;
Global Telecommunications Conference, 1993, including a Communications Theory Mini-Conference. Technical Program Conference Record, IEEE in Houston. GLOBECOM '93., IEEE , 29 Nov.-2 Dec. 1993
Pages:1501 - 1505 vol.3

[Abstract] [PDF Full-Text (396 KB)] IEEE CNF

h eee e eee g e ch e ch e e c e e e